Changes Approved 4/13/05 JBL

AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 6, line 17 with the following amended paragraph:

The ORC effectively branches to a digital clocking system 116 and to one or more analog clocking systems 122. The digital clocking system 116 consists of a timing path that includes a first frequency divider 118 for dividing the ORC by an integer "D" to produce a first digital output clock C0 (also designated as c0 in FIGS. 3 to 9). A second divider 120 divides the first digital output clock C0 by an integer "J" to produce a second digital output clock T0 (also designated as t0 in the FIGS. 3 to 9). Digital clocks C0 and T0 can then be used to control the timing of digital vectors applied to or sampled from the DUT. The analog clocking system 122 includes four timing paths. Each timing path includes a first frequency divider 124 (DMC_0 – DMC_3) for generating a respective analog master clock (AMC_0 – AMC_3), a multiplexor (any of 126a – d) for directing the output of the first frequency divider, and a second frequency divider 128 (DA_0 – DA_3), for generating a respective output clock (A_0 – A_3) (designated as a0- a3 in the FIGS. 3 to 9). The output clocks A_0 – A_3 are transmitted over an instrument bus, where they are accessible for use by individual instruments.

Please replace the paragraph beginning at page 7, line 3 with the following amended paragraph:

Fig. 2 illustrates a tester environment in which the invention may be used. A user 210, for example a test engineer, operates a workstation or other computer 212. The workstation 212 runs a computer program 213 for configuring clocks in a tester 220 and a test program 218. The tester 220 includes a clocking system 222, which corresponds to the clocking system 100 of Fig. 1. The tester 220 also includes digital I/O 224, for sourcing and sampling digital signals from a DUT 228 under control of clocks C0 or T0, and analog instruments 226 ~~224~~, for sourcing and sampling analog signals under control of the analog clocks $A_0 - A_3$.

Please replace the paragraph beginning at page 13, line 6 with the following amended paragraph:

The Instrument Form 700 simplifies the task of ensuring coherence by allowing the user to configure one instrument's timing characteristics as a function of another instrument's timing characteristics. Clicking buttons 726, 728 and 730 ~~326, 328, and 330~~ on the Instrument Form causes the form to display additional fields for configuring timing dependencies for F_s, F_i, and F_{res}, respectively.

Please replace the paragraph beginning at page 13, line 26 with the following amended paragraph:

The contents of the calculator region 900 are substantially identical regardless of which of the buttons 726, 728 and 730 ~~326, 328, and 330~~ has been clicked, with the exception that the title of the calculator region is changed based on the button pressed. The title reads, "F_s

Dependence" when button 726 is clicked, "F_i Dependence" when button 728 is clicked, and "F_{res} Dependence" when the button 730 is clicked.

Please replace the paragraph beginning at page 14, line 22 with the following amended paragraph:

It is significant that the LCM is the "least" common multiple, rather than some other common multiple, of the desired frequencies and the master clock. Making the LCM the "least" common multiple maximizes the flexibility with which the algorithm can distribute divisions among different tiers of dividers in the clocking system (i.e., first dividers 124 and second dividers 128). This is important because the Analog Master Clocks ($AMC_0 - AMC_3$) in the *Catalyst* test system have an upper and a lower frequency limit. Therefore, the second dividers 128 (DA_L) must be chosen so that the desired frequencies F_{DES-L} times the second dividers DA_L fall within the allowable range of the AMCs. In addition, if the LCM is greater than the maximum allowable ORC (2^{29}), no solution ~~can set~~ will enable the clocking system to precisely produce the desired frequencies. Finding the "least" common multiple thus affords the algorithm its highest probability for success.

Please replace the paragraph beginning at page 16, line 7 with the following amended paragraphs:

In variable ORC mode, coherency grouping need not be considered because the flexibility of varying the ORC obviates the need for rounding. Since frequencies are not

rounded, frequency ratios are preserved across all clocks, whether coherence is required or not.

Referring now to Fig. 11, the first ~~three~~ four steps 1110 – 1114 for fixed ORC mode are closely related to steps 1010 – 1014 of Fig. 10. At step 1110, the algorithm seeks as before to find the least common multiple (LCM) of the desired frequencies and the frequency of the master clock, i.e., the LCM of $A_0 - A_3$, C0, and 100 MHz. At step 1111, however, the algorithm also seeks to find a larger least common multiple, "BigLCM," of the desired frequencies and the ORC, i.e., the LCM of $A_0 - A_3$, C0, and 50,000 THz. BigLCM is then used at step 1112, wherein the second dividers are chosen to minimize new factors beyond those already included in BigLCM. The factors of BigLCM are relevant, instead of those of LCM, to allow the algorithm to find, whenever possible, divider values that exactly produce the desired frequencies (i.e., without rounding—see below). Note that BigLCM is used only for minimizing new factors in step 1012. Once the new factors, if any, are determined, the algorithm calculates LumpLCM as the product of LCM any additional factors needed to realize the second dividers.